



PTO/SB/08A (07-05)

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Substitute for form PTO 10 Modified <div style="text-align: center;">INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)</div>	<div style="text-align: right;">Complete if Known</div> Application Number 10/700,033 Confirmation No.: 3398 Filing Date: November 3, 2003 First Named Inventor: Gregory William Smaus Art Unit: 2183 Examiner Name: Cody, Dillon J. Attorney Docket Number: 5500-91600
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Sheet 1 of 2

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code (if known)			
BJ		US-2004/0143721	7/04	Pickett, et al.	
BJ		US-7,003,629	2/21/06	Alsup	
BJ		US-6,247,121	6/01	Akkary, et al.	
BJ		US-3,896,419	7/75	Lange, et al.	
BJ		US-5,381,533	1/10/95	Peleg	
BJ		US-6,449,714	9/10/02	Sinharoy	
BJ		US-6,339,822	1/15/02	Miller	
BJ		US-6,256,727	7/3/01	McDonald	
BJ		US-6,185,675	2/6/01	Kranich, et al.	
BJ		US-6,345,295	2/02	Beardsley, et al.	
BJ		US-5,930,497	7/99	Cherian, et al.	
BJ		US-6,578,128	6/03	Arsenault, et al.	
BJ		US-6,973,543	12/05	Hughes	
BJ		US-6,823,428	11/23/04	Rodriguez, et al.	
BJ		US-6,167,536	12/00	Moann	
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BJ		US-2002/0144101	10/02	Wang, et al.	
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BJ		US-2004/0083352	4/04	Lee	
BJ		US-2004/0193857	9/04	Miller, et al.	
BJ		US-2005/0125632	6/05	Alsup, et al.	
		US-			

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	Check if English Translation is attached
		Country Code-Number-Kind Code (if known)				
BJ	A1	GB 2 281101	4/23/03			<input type="checkbox"/>
BJ	A2	EP 0 957 428	11/17/99			<input type="checkbox"/>

Examiner Signature	/Brian Johnson/	Date Considered	08/26/2006
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Substitute for form 1449/PTO Modified		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(Use as many sheets as necessary)</i>		Application Number	10/700,033
		Confirmation No.:	3398
Sheet 2 of 2		Filing Date:	November 3, 2003
		First Named Inventor:	Gregory William Smaus
		Art Unit:	2183
		Examiner Name:	Cody, Dillon J.
		Attorney Docket Number:	5500-91600
NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, (page(s), volume-issue number(s), publisher, city and/or country where published.	Check if English Translation is attached
BJ	A3	Yuan Chou, et al., "Instruction Path Coprocessors," March 2000, pp. 1-24.	<input type="checkbox"/>
BJ	A4	Friendly, et al., "Putting the Fill Unit to Work: Dynamic Organizations for Trace Cache Microprocessors," Dept. of Electrical Engineering and Computer Sciences, The Univ. of Michigan, December 1998, 9 pages.	<input type="checkbox"/>
BJ	A5	Bryan Black, et al., "Turboscalar: A High Frequency High IPC Microarchitecture," Dept. of Electrical and Computer Engineering, Carnegie Mellon Univ., June 2000, pp. 1-	<input type="checkbox"/>
BJ	A6	Rotenberg, et al., "Trace Cache: A Low Latency Approach to High Bandwidth Instruction Fetching," April 11, 1996, pp. 1-48.	<input type="checkbox"/>
BJ	A7	Merten, et al., "An Architectural Framework for Run-Time Optimization," June 2001, pp. 1-43.	<input type="checkbox"/>
BJ	A8	Jourdan, et al., "Increasing the Instruction-Level Parallelism through Data-Flow Manipulation," Intel, 11 pages.	<input type="checkbox"/>
BJ	A9	Hinton, G., et al., "A 0.18-MUM CMOS IA-32 Processor with a 4-GHZ Integer Execution Unit," IEEE Journal of Solid-State Circuits, Vol. 36, No. 11, November 2001, pages. 1617-1627.	<input type="checkbox"/>
BJ	A10	Sanjay J. Patel, et al., "replay: A Hardware Framework for Dynamic Optimization," IEEE, Vol. 50, No. 6, June 2001, pp. 590-608.	<input type="checkbox"/>
BJ	A11	Jacobson, et al., "Instruction Pre-Processing in Trace Processors," IEEE Xplore, January, 1999, 6 pages.	<input type="checkbox"/>
BJ	A12	Bryan Black, et al., "The Block-Based Trace Cache," IEEE, 1999, pp. 196-207.	<input type="checkbox"/>
BJ	A13	Rotenberg, et al., "Trace Cache: a Low Latency Approach to High Bandwidth Instruction Fetching," IEEE, 1996, pp. 24-34.	<input type="checkbox"/>
BJ	A14	Grant Braught, "Clas #21-Assemblers, Labels & Pseudo Instructions," Dickenson College, Fall Semester 2000, 6 pages.	<input type="checkbox"/>
BJ	A15	Patterson, et al., "Computer Architecture A Quantitative Approach," Second Edition, Morgan Kaufmann Publishers, Inc., 1996, pp. 271-278	<input type="checkbox"/>
BJ	A16	Palmer, et al., "Fido: A Cache That Learns to Fetch," Proceedings of the 17 th International Conference on Very Large Data Bases, Barcelona, September 1991, pp. 255-264.	<input type="checkbox"/>
BJ	A17	Chen et al., "Eviction Based Cache Placement for Storage Caches," USENIX 2003 Annual Technical Conference, (13 pages)	<input type="checkbox"/>
			<input type="checkbox"/>

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